



Sri

SAIRAM

COLLEGE OF ENGINEERING

Anekal, Bengaluru

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

DATE: 13.11.2021

Accredited by NAAC

ISO 9001:2015 Certified Institution

Approved by AICTE, New Delhi

Affiliated to Visvesvaraya Technological University

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REPORT

ON

GUEST LECTURE - ON "VLSI DSP ARCHITECTURES"

The Department of Electronics and Communication Engineering, Sri Sairam College of Engineering Organized Guest lecture on "VLSI DSP ARCHITECTURES" from 12th November 2021 @ 11.15am to 12.45p.m through online Zoom Platform.

The guest lecture was inaugurated by the welcome speech by **Dr.T.N. Prabakar**, Head of the department ECE also Sir introduced the speaker of the day. Our beloved **Dr.B. Shadaksharappa**, Principal Sri Sairam College of Engineering conveyed the best wishes for organizing such guest lectures.

The **resource person Dr.G. Seetharaman**, Head of Department of ECE, IIIT, Tirchy. Sir has given insight about VLSI Design, design of Braun Multiplier and insight of FPGA architecture and how it used in design of digital systems and detailed talk about the various opportunities in emerging field of VLSI. Very interesting delivery. Around 60+participants joined the session. The important take away of the session was the students learnt about the practical aspects about VLSI design and DSP Architectures.

The vote of thanks to the speaker was given by **Prof. Aruna R**, Assistant Professor, ECE, Sri Sairam college of Engineering.

Coordinator
(Prof.Santosh Kumar N)

HOD
(Dr.T.N. Prabakar)

PRINCIPAL
Dr.B.SHADAKSHRAPPA



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Department of
ELECTRONICS & COMMUNICATION ENGG.
organizes



Guest Lecture on
“VLSI DSP Architectures”
12th November 2021 @11:15 am

Speaker



Dr. G. Seetharaman

Head of Department, Associate Professor
IIT, Tiruchy

Prof. Santosh Kumar N
Coordinator

Dr. T N Prabakar
Prof. & HOD, ECE

Dr. B. Shadaksharappa
Principal

Sri Sai Prakash LeoMuthu
Chairman & CEO, Sairam Institutions





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FPGA Architecture

Dr. G. Seetharaman,
Department of ECE/IIT

1

03:15 -1:21:08
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6

17:22 -1:07:01

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Introduction (cont'd)

- Example 1:** Consider a 3-tap FIR filter: $y(n) = ax(n) + bx(n-1) + cx(n-2)$

T_M : multiplication – time
 T_A : Addition – time

- The critical path (or the minimum time required for processing a new sample) is limited by 1 multiply and 2 add times. Thus, the “sample period” (or the “sample frequency”) is given by:

$$T_{sample} \geq T_M + 2 T_A$$

$$f_{sample} \leq \frac{1}{T_M + 2 T_A}$$

1:05:34 -18:49

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