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Analysis of Power Quality Progress in Hybrid Cascaded H-Bridges Multilevel Inverter

Dr. Keshav Patidar[1], Dr. T G Manjunath[2], Dr. T. Guhan[3], Dr. T N Prabakar[4], Abhijeet M. Dhulekar[5], Rajesh A S[6]

[1]Electronics and Communication Engineering, Indore institute of Science and technology, Madhya Pradesh - 453331
[2]Electrical and Electronics Engineering, Sai Vidya Institute of Technolgy, Karnataka -560064
[3]Computer Science and Engineering, Sri Ramakrishna Engineering College, Tamilnadu - 641022
[4]Electronics and Communication Engineering, Sri Sairam College of Engineering, Karnataka -562106
[5]Mechanical Engineering, P. R. Pote (Patil) College of Engineering and Management, Maharashtra- 444602
[6]Mechanical Engineering, JSS Science & Technology University, Karnataka -570006
[1]keshavpatidar1@gmail.com, [2]tgmnath@gmail.com, [3]tg@srec.ac.in, [4]tnprabakar@gmail.com, [5]dhulekarabhijeet@gmail.com, [6]as.rajesh.jce@gmail.com

Abstract-
In the new years the staggered inverters were generally talked about theme for scientists. In view of not many benefits of having great force quality. Fundamentally inverter is a converter, which is skilled in changing over the DC power into AC power at wanted level. The two level yields, zero or positive or negative V dc can be gotten by voltage source inverter (VSI). The staggered inverter is skilled to create sinusoidal yield voltage and to decrease Complete Symphonious Bending at wanted voltage level. As we increment the degree of voltage, the yield power quality gets improved, for example THD gets diminished. This paper proposes the execution and investigation of fell staggered inverter with decrease THD. The executed Fell H-span Staggered Inverter geography is a useful geography; it gives the summed up way to expand the degree of staggered inverter as we need. In the addressed model of eleven level single stage Fell H-span Staggered Inverter has been planned utilizing IGBT to produce the diverse yield voltage levels at legitimate stretches, the conduction point of IGBTs have been constrained by fluctuating the beat width of getting signals. Re-enactment models are created in MATLAB-SIMULINK of eleven levels inverters and THD examination is performed.

Keywords: *A2D Converter, Total Harmonic Distortion, Hybrid Multilevel Inverter, Diode Clamped Multilevel Inverter, CNN.*

1 INTRODUCTION

The effects of various modulation methods for hybrid inverters are compared. Multilevel inverters are controlled using DSP-based multicarrier pulse width modulation methods such as PDPWM, PODPWM, and APODPWM. All of these modulation methods have been tailored for specific HMLI, which are often used in cascaded multilevel inverters, symmetrical or asymmetric hybrid multilevel inverters, or other multilevel inverters. As a result, all of these modulation methods are unique to this project[1]. The system is controlled using a mix of MATLAB/SIMULINK, CCS, emulation, and DSP. The software-based control system designed for hybrid Multilevel Inverter system optimization allows for configuration modifications and future development. The paper discusses the use of various modulation methods, as well as modelling, analysis, and implementation of hybrid multilevel inverter control. THD is compared in simulations for single phase cascaded five level multilevel inverters. THD is calculated for simulated circuits with modulation for single phase and three phase topologies using various modulation methods [2]. The chosen hybrid multilevel inverter is available in single phase and three phase configurations. Multicarrier modulation

methods such as PD, POD, and APOD are used in the project with a fixed modulation index that may be adjusted to obtain various effects [3]. This system can handle a motor with a power output of 1.0 HP. This promotes the adoption of sophisticated control techniques in controller design and development. The scalar control technique is simple to implement and produces excellent results over a wide speed range, but it has a slow reaction owing. For the fulfilment of necessary information, specifications are gathered and provided. The most suitable board is chosen based on whether or not its specifications match those of our application[4]. The ability to connect with our power circuit and interface with our control circuit is tested using ADC, PWM, and encoder linkage. This is investigated using data sheets from a manufacturing firm[5]. The evaluation board's interfaces, such as three-phase PWM, Analog-to-Digital conversion, and so on, are evaluated before the control system is implemented.

2. RELATED WORKS

We did a study on power circuit for induction motor based on multilayer inverter before beginning work on this area of embedded goal design[6]. Three-level inverters are often employed in power systems and power electronics applications, according to the literature. This circuit has three levels. For low voltage applications, control strategies like as SPWM, SVPMW, and selective Harmonic elimination techniques are utilised[7]. However, thanks to the development of the multi-level inverter, power modules for power electronics may now be utilised at medium and high voltages[8]. The level of a multilayer inverter may run up to 27 or more for power system applications like FACTS and HVDC, but for medium voltage applications like induction motor driving, five and seven levels are adequate. Following the completion of the levels, a study of several multilevel topologies such as diode clam, flying capacitor, and cascaded H- Bridge MLI is conducted to determine the advantages and disadvantages of each topology[9]. Following a review of different topologies, we discovered that the Hbridge topology may be used for drives[10]. Simultaneously, we want to minimise the number of switches in MLI. Following a review of several research papers, we chose the Hybrid MLI architecture[11]. However, we subsequently discover that DSP 2812 is a fixed point DSP, and that it performs poorly when utilised for FOC, where a significant amount of mathematics is needed for different transformations such as Park and Clerk. We go from fixed point DSP 2812 to floating point DSP 28335, with the goal of providing a standard plate-form for any kind of control technique for induction motor drives[12]. Following a review of the literature, we find that developing a programme in C or assembly language to implement the control algorithm on an embedded target is time consuming and error prone[13]. Some tools, like as dSPACE, Lab-view, and Real-Time Workshop, are now available for generating code from a ready-made block set to an embedded target. Here, we utilise RTW in conjunction with an IDE environment such as Code Composer Studio CCS to generate code[14].

3. PROPOSED METHODOLOGY

The carrier-based PWM methods for cascaded multilevel inverters may be divided into two categories: phase shifted modulation and level shifted modulation, in which the carrier waves are moved in amplitude and phase. [15][16]. For signal production in both methods, (n-1) triangular carrier waves are required for the ‘n' level inverter. All carrier waves should have the same frequency and peak to peak magnitude to occupy contiguous bands throughout the range +Vdc to –Vdc.

3.1 Level Shifted Multicarrier pulse width modulation technique

Level-Shifted multicarrier modulation may be done in three ways: - i. IPD (In Phase Disposition): All of the carriers in this modulation[17]. At least four levels were needed in a five-level inverter. Figure 1 depicts the carrier wave in the IPD modulation method. A switching signal is produced based on the amplitude of the reference signal in relation to the carrier.

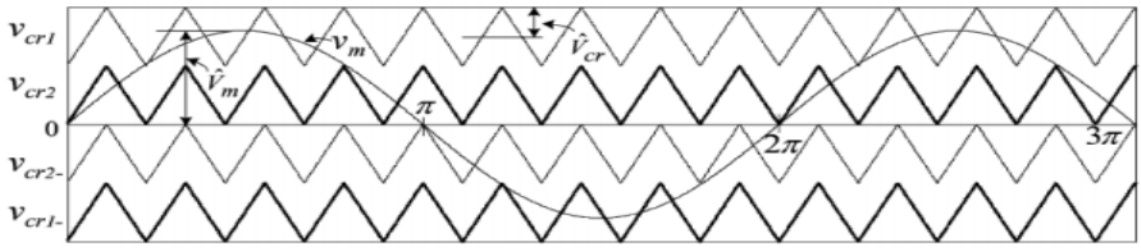

Figure 1-PWM in Phase Disposition for a 5-level CHB inverter

As a result of phase opposition modulation, carrier waves above the sinusoidal zero reference line are in phase, while carrier waves below the zero reference line are 180 degrees out of phase as compared to the carrier wave above the zero line[18-20]. In terms of Vcr1 and Vcr2, as shown in fig.2, Vcr1 and Vcr2 are in phase, while Vcr1- and Vcr2- are in phase opposition.

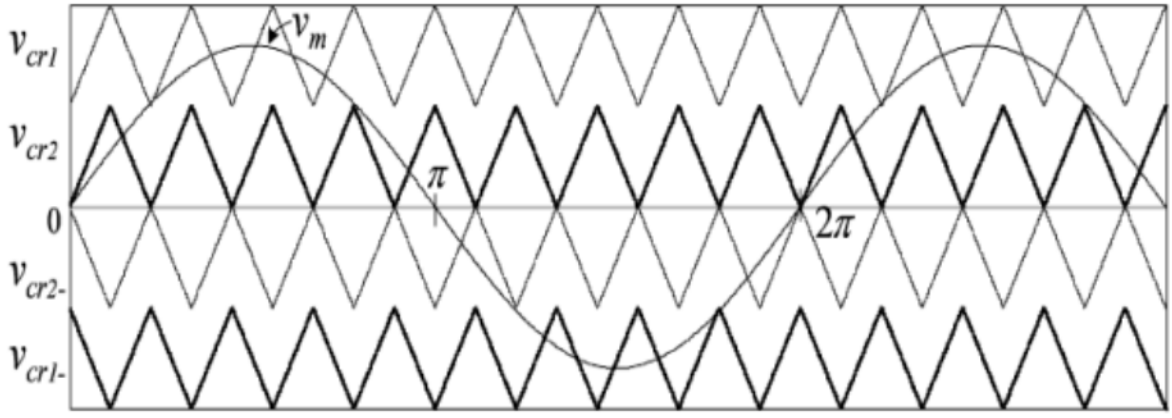

Figure 2-Phase Opposition Disposition PWM for 5-level CHB inverter

Alternate phase opposition disposition (APOD) modulation is a modulation technique in which each carrier is 180 degrees out of phase with its neighbouring carrier. Figure 2 shows the carrier and reference wave configurations for a 5-level inverter that is modulated using the APOD modulation technique, as shown in the figure. In phase opposition, Vcr1 and Vcr2 are 1800 above the zero line, while Vcr1- and Vcr2- are 1800 below the zero line, indicating that they are in phase opposition. One definition of asymmetrical topology is two H- Bridges cascaded together with two voltage sources of different magnitudes. It is possible to utilise a variety of voltage-rated switches in this application, each of which may operate at a particular voltage level and frequency. High voltage and low switching frequency are used in the upper bridge, while low voltage and high switching frequency are used in the lower bridge. Figure 1 shows the difference between the two bridges. As a consequence, we selected GTO for the H-bridge on the higher level and IGBT for the H-bridge on the lower level[21]. With this configuration, we can take use of all of the switches' capabilities. However, the major disadvantages of this topology are the two D.C sources and the complexity[22-24]. H-bridge having several switch types, such as GTO and IGBT. However, the triggering circuit becomes

complicated as a result of this arrangement, and it is built for various voltage and current ratings for each device. After looking at the table above, we can see that another topology with the lowest THD is the symmetrical H bridge topology. However, in this configuration, eight switches of the same kind are needed, as well as two separate DC supplies. As a result, we completed our architecture with six switches in each leg, as shown in the table. The upper bridge is a complete bridge with a high switching frequency, while the lower bridge is a half bridge with a low switching frequency.

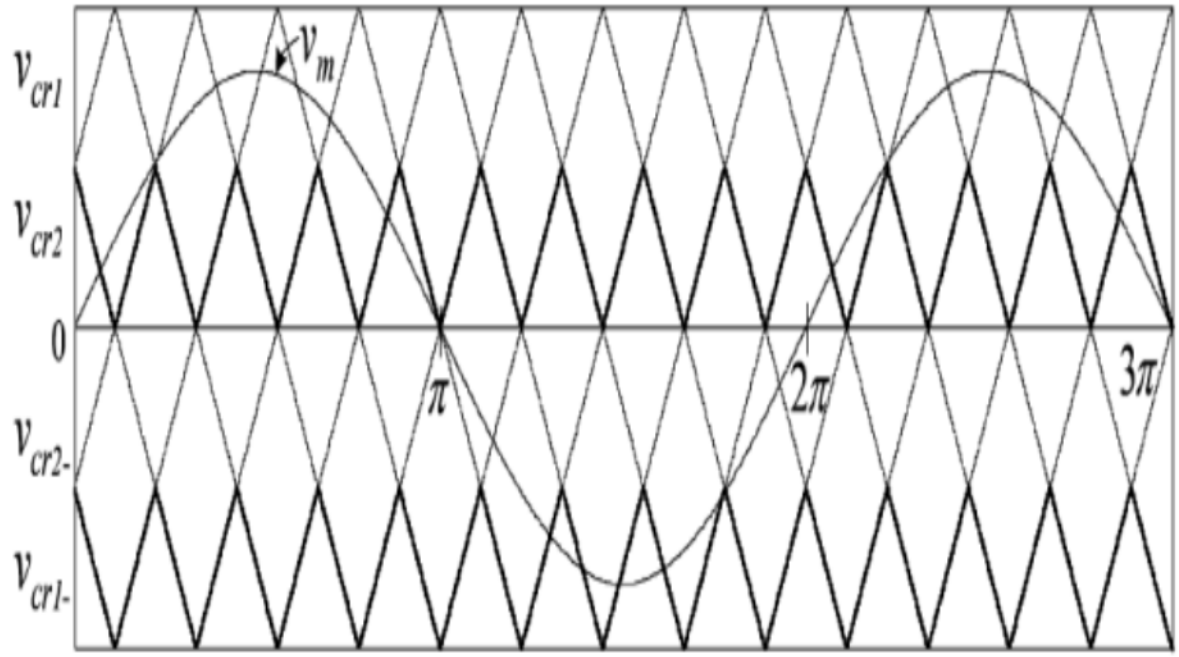

Figure 3-PWM for 5-level CHB inverter with alternate phase opposition disposition

APOD (alternative phase opposition disposition): In this modulation method, each carrier is 180 degrees out of phase with its neighbouring carrier[25-28]. Figure 3 depicts the carrier and reference wave arrangements for a 5-level inverter using the APOD modulation method. Vcr1 and Vcr2 are 1800 above the zero line in phase opposition, while Vcr1- and Vcr2- are 1800 below the zero line in phase opposition[29].

3.2 Phase Shifted Multicarrier pulse width modulation technique

There is a phase difference between subsequent two carrier waves equal to cr = 3600 /(n-1), where n is the number of levels in the output. In Phase Shifted Multicarrier Modulation Technique, all triangular carriers have the same frequency and peak-to-peak amplitude, but there is a phase difference between subsequent two carrier waves equal to cr = 3600 /(n-1). As the modulating signal, it is common to utilise a three-phase sinusoidal wave with variable amplitude and frequency characteristics[30]. The modulating wave and the carrier waves are compared to generate gate signals, as shown in Fig. 4. This topology is known to as an asymmetrical topology due to the fact that two H- Bridges are cascaded with two different magnitudes of voltage sources in this configuration. It is possible to utilise a variety of voltage-rated switches in this application, each of which may operate at a particular voltage level and frequency. High voltage and low switching frequency are used in the upper bridge, while low voltage and high switching frequency are used in

the lower bridge. Figure 1 shows the difference between the two bridges[31]. As a consequence, we selected GTO for the H-bridge on the higher level and IGBT for the H-bridge on the lower level. With this configuration, we can take use of all of the switches' capabilities. The two direct current sources and the intricacy of this topology, on the other hand, are its main drawbacks. One advantage of this design is that it necessitates the use of fewer switches[32]. The modular multilevel inverter is composed of three half-bridge modules that are linked in series to form the inverter. These modules are connected together in a delta configuration to form a three-phase system, and the DC link capacitors do not need a separate DC power source to function. The consequence is a little capacitor imbalance, which we're dealing with here. This kind of inverter requires a larger number of insulated DC sources than a CHB in order to achieve the same number of levels. The DC sources, on the other hand, operate at lower levels of active power consumption is shown as figure 4 and 5.

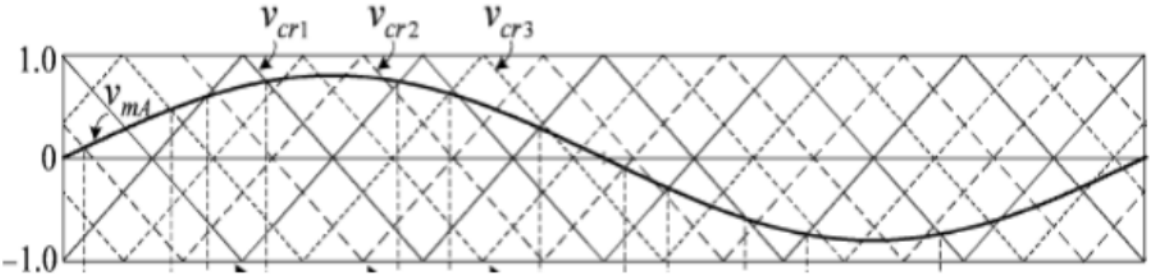

Figure 4-PWM with phase shift for a 5-level CHB inverter

Table 1-PWM Techniques Based on Multicarriers: A Comparison of Level Shifted and Phase Shifted Techniques

COMPARISION	PHASE SHIFTED MOD.	LEVEL SHIFTED MOD
SWITCHING FREQ.	SAME FOR ALL DEVICE	DIFFERENT
CONDUCTION PEIOD SAME	SAME FOR ALL DEVICE	DIFFERENT
THD (L-L)	GOOD	BETTER.

4. RESULT AND DISCUSSION

In this section of the paper, we simulated one of the HMLI configurations using several modulation methods and compared the results. We compared the PD, POD, and APOD results here.

Technique for simulating POD modulation:

- Figures 6 and 7 illustrate a simulation circuit for POD, as well as its gate signal and output voltage waveform.

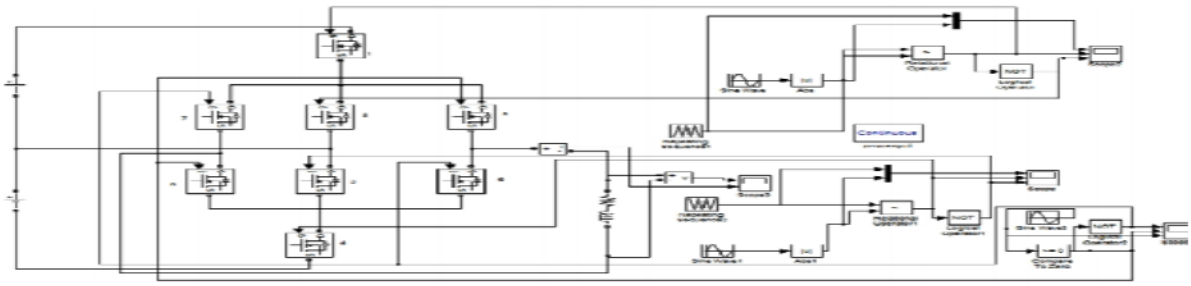

Figure 5- Simulation Model of 5 level HMLI using SPWM with R-L Load POD modulation

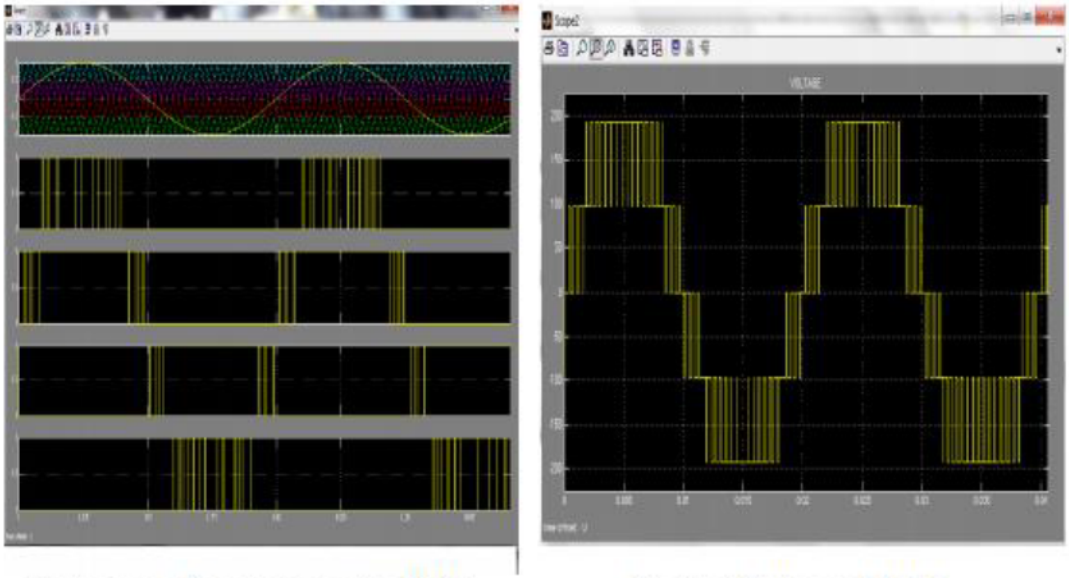

Figure 6- Simulation Results: POD

Generally V/F, Direct torque control technique (DTC), and field oriented control method (FOC) are the most common speed control methods for induction motors[33][101-103][33-34]. We used the v/f speed control technique [34] for this study. This technique was chosen because it is simple to implement. As a result, speed control is not a major focus in this essay. Implementation of a speed control technique

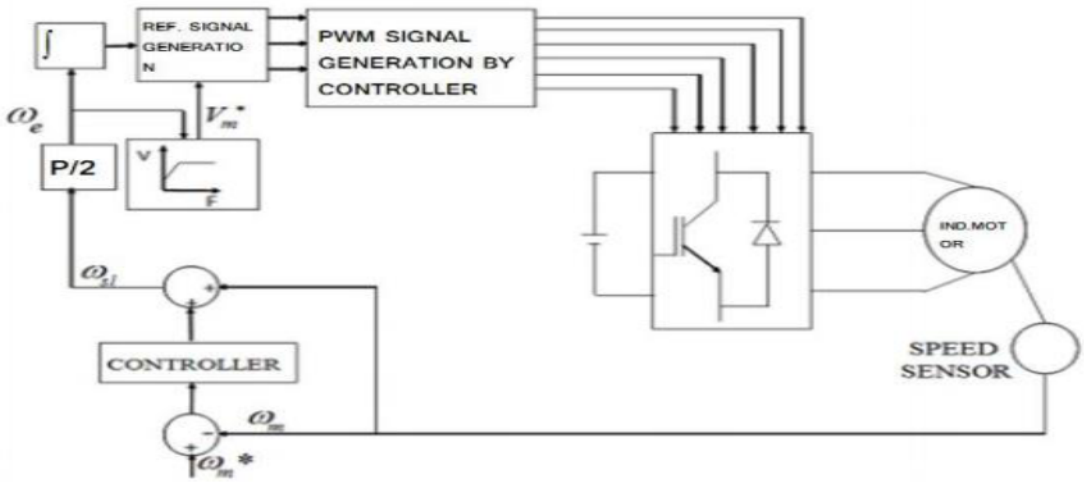

Figure 7-V/F technique block for Induction Motor Drives with Variable Frequency Speed Control

The encoder detects the speed and compares it to the reference speed. The PI controller is used to handle the error signal. The PI controller's output is combined with the real and synchronous speeds. A mechanical degree of synchronous speed is produced as a result of this. This output is multiplied by a pole pair to create an electrical speed that is comparable to mechanical speed. To determine the electrical location of the rotor, an electrical speed signal is incorporated. At the same time, the peak value of voltage Vm corresponding to the rotor position is retrieved from a look-up table. The suggested system is split into four components, as illustrated in the block diagram in fig 8. In chapter 4, the first portion of hardware is covered, which is linked to loading a programme into a DSP through JTAG with the aid of RTW, embedded coder, MATLAB Simulink, and CCS IDE. The second phase involves detecting signals like as current, voltage, and speed and conditioning them to make them compatible with DSP. The control signal generated by the DSP 28335 is sent to the inverter module through an isolator circuit in the third component. The loading of an induction motor through a DC generator via a loading panel is the fourth component of this hardware configuration.

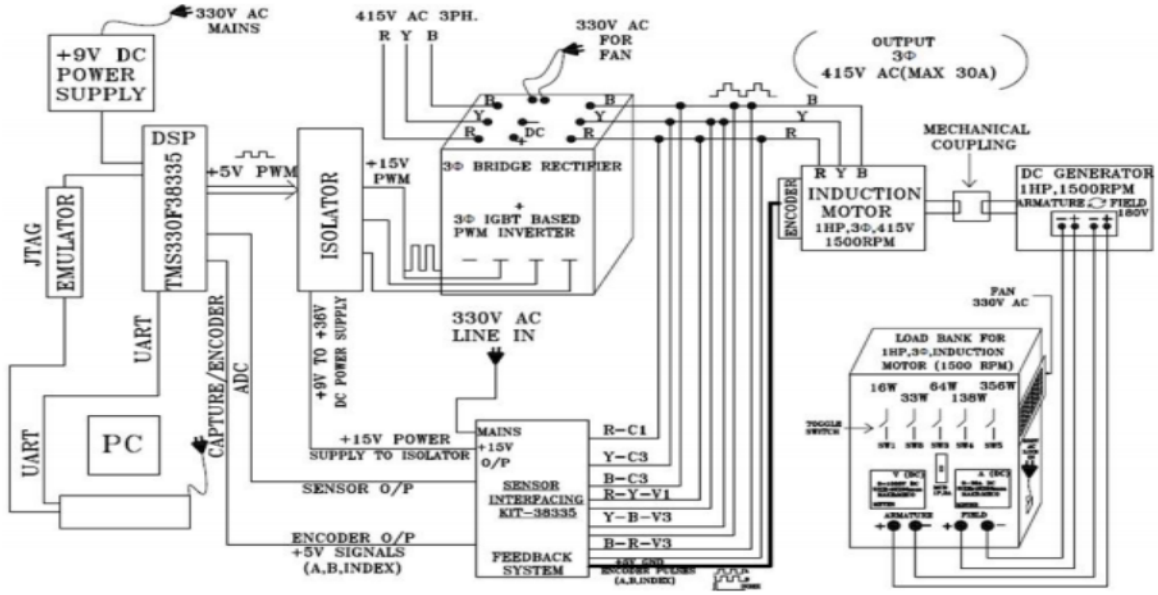

Figure 8-Overall hardware Set-up for induction motor drives.

As illustrated in Figure 8, the output current of the motor is detected by the current sensor LEM LA25NP, and the voltage is sensed by the voltage sensor LEM LV 25P. The hall effect is used in both of these sensors. This current and voltage sensor has the benefit of providing isolation between the power and control circuits, as well as high accuracy. The analogue output is in the range of 15V using a voltage sensor and a current sensor with an appropriate resistance. As a result, the voltage level of the sensor output must be converted to be compatible with the DSP, which is in the range of 0V to +3.3V. LEM LA 25NP converts current signals into voltage. Similarly, the input voltage to the LEM LV 25P is first scaled down using a 10K resistor. However, to achieve isolation, the voltage must be reduced to less than 15 volts. As a result, six channels have been established. An operational

amplifier with low noise, high slew rate, and high common mode rejection ratio is required for effective signal conditioning (CMRR) To save space, an integrated package of four op-amps[35] was used.

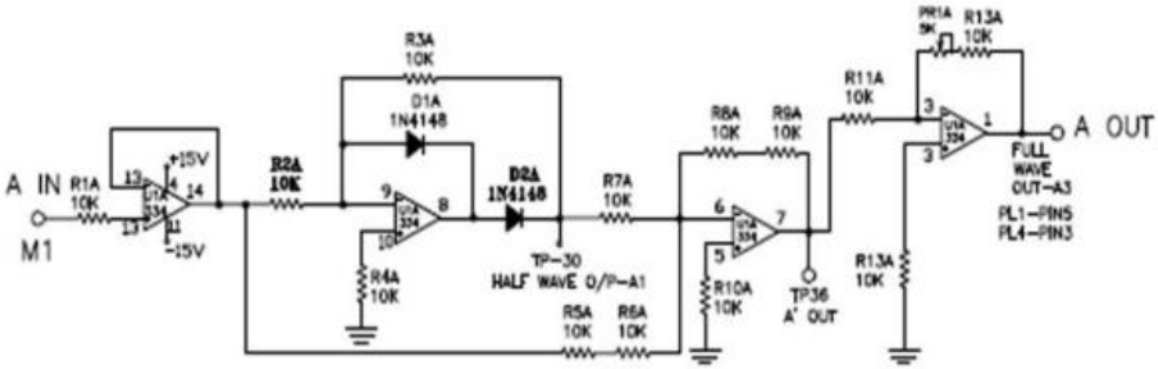

Figure 9-Conditioning circuit for ADC

In Fig. 9, the first Op-Amp is set as a voltage follower with a high input impedance in order to minimise the loading effect of the source signal on the first Op-Amp. The second operational amplifier converts the output of the first stage to a unidirectional half wave voltage at its output. A full wave and shifted output is produced by the third operational amplifier, which converts and adds the output of the second operational amplifier, while simultaneously serving as a summer. This results in a full wave and shifted output from the third operational amplifier. The third operational amplifier's output voltage is scaled down to 0V to 3.3V so that it may be delivered directly to the DSP. It has already been established that the DSP F28335 is compliant with the LVTTL standard, which is not the same standard as the TIA-422-B standard. There are several different types of receiver integrated circuits (ICs) available for converting TIA-422 to LVTTL. In order for a voltage divider to be effective, it must be set at a voltage level that is compatible with the DSP's input. The output voltage at the highest setting should be 4.4V. In terms of voltage range, the F28335 DSP can handle voltages up to 3.3V [23]. Because of this, the resistance fractional ratio was selected such that the DSP would operate at 3.3 V. Fig. 9 shows how the encoder signals are sent into the interface board via a 15-pin D-Sub connection DB-15 that has the same pin arrangement as the DSP and is connected to the interface board.

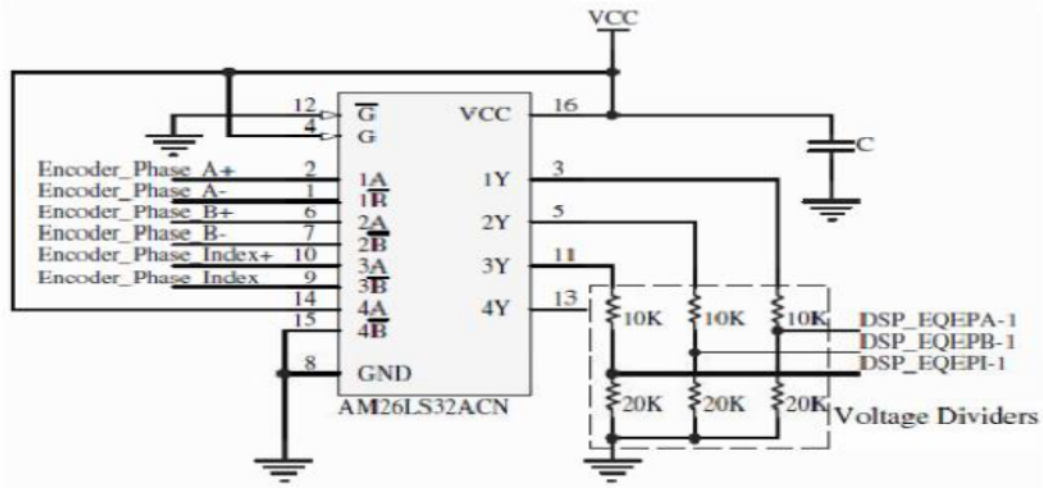

Figure 10-Circuit schematic for encoder interface

Above Figure 10 shows that Isolation is needed in power electronics because certain parts of the power circuit work at hundreds of volts while the control circuit operates at tenths of volts. To protect the embedded controller from overvoltage damage, the connection between the two must be separated. Direct contact is not needed. Of course, relays can offer this isolation, but even tiny relays are large in comparison to ICs and many of today's other micro circuit components. They are unreliable and unsuitable for low-speed operation since they are electromechanical. We may also utilise the pulse transformer for restricted control signals for isolation purposes. Optical isolators are useful when a compact size, excellent dynamic speed response, and better dependability are needed. The data is transferred via an optical barrier, which provides excellent isolation. Because the power circuit in power electronics operates at a voltage of kV and the signals used for device triggering are at a voltage of up to 10V, optical isolation is the best option. Pulse transformers and optical isolation are two typical isolation circuits, which will cause the photo detector's LED to light up and glow, which will cause a corresponding electrical signal to be produced in the output circuit. Photodiode detectors produce current that is proportional to the amount of incoming light they receive from the emitter. Opto isolator with a single channel and high speed, the MCT6 is designed for use in high-speed systems. Designed for high-density applications, the MCT6 is a two-channel opto coupler with an output voltage of 3.3V. In each channel, an infrared LED made of gallium arsenide and silicon NPN phototransistors are connected optically. In addition to being designed especially for driving medium-speed logic, the MCT6 may be used to minimise ground loop and noise problems. The device may also be used to replace relays and transformers in a variety of digital interface applications.

5. CONCLUSION

Based on the research given above, we believe that the V/F technique is the best to apply, although it is the least important for our project. However, using this arrangement, we may experiment with other speed control methods. We may relieve the difficult technique of manual code writing by using the CCS integrated environment in combination with real time workshop (RTW) and embedded coder. By using auto-mated code creation, we were able to get a result that was comparable to simulation. Writing typical code for embedded processors DSP 2812 and 28335, which is extremely complicated, takes several hours and days. Here, we'll look at some of the blocks we'll need to include in our programme, such as analogue digital blocks, PWM blocks, and capturing modules. This setup demonstrates that the control technique used for MLI in this study yields the same results. As a result, we may use the same code generating approach for various modulation methods.

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