

Digital space vector modulation decoupled control scheme grid connected 1- \emptyset riven bias inverter to suppress high-frequency current commutation

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Abstract

A single-juncture topology of 3- \emptyset boost inverter with riven DC supply configuration grieves from larger incidence current commutations across the diode_{passive} in connection with the DC source and the intricate study as the inductor charges with capricious duty cycle. This study focuses on 1- \emptyset riven bias inverter with improvised technique on inverter and modulation. The riven bias inverter is analyzed using state space averaging technique to derive the mathematical model that is suitable for both steady-state and dynamic behavior conditions considering main converter nonlinearities. Hence, the research is carry forwarded in modeling the riven bias inverter on DC section with digital space vector modulation control technique to obtain decoupled control structure in lattice network and the work is validated by means of MATLAB/SIMULINK.

Keywords

Riven bias inverter, digital space vector modulation, battery energy storage system

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Introduction

Abeywardana et al.¹ confined the analysis toward the method that reduces the second-order harmonics on the DC current of single-phase grid-connected inverter-based energy storage system (ESS). Lee et al.² proposed the analysis of genetic algorithm (GA) in optimizing the switching angle of multilevel boost inverter with integrated battery energy storage system (BESS) for stand-alone grid tie system. In addition, the designed inverter topology is compared with the conventional topology with respect to cost, reliability, and elimination of lower order harmonics. Diab et al.³ proposed the novel modulation technique capable of operating at high-voltage gain without added hardware in Z-source inverter (ZSI) to enhance the boosting capability and to control the shoot through periods in ZSI. Siwakoti et al.^{4,5} dealt with the review of various impedance source grid (ISG)-based power converter analysis with various modulation techniques. Sahan et al.⁶ focused on the development of technology used in optoelectric source that led to the rigorous investigation in electrical energy translation system. The use of inverter and its modulation technique is the most enabling technology in the integration of nonconventional energy sources. Abdelhakim et al.⁷ proved that the split source inverter has incessant DC link voltage, unremitting input current, low-voltage stress with high-voltage gain, and typical modulation technique⁸⁻¹¹ and have discussed three-level diode clamped and flying capacitor operation with modulation technique.

Stimulated by the introductory effort, this research work proposes a novel single-phase version of riven bias inverter (RBI) with improvised inverter and modulation technique. The RBI is analyzed using state space averaging technique to derive the mathematical model that is suitable for both steady-state and dynamic behavior conditions taking main converter nonlinearities. Hence, the research is carry forwarded in modeling the RBI on DC section with digital space vector modulation (DSVM) control technique to obtain decoupled control structure in lattice network. The modulation technique designed works in all states without any nonzero states. The inductor is charged with the constant duty ratio, and high-frequency commutation is avoided across the diodes.

The technical exploration in this study helps the undergraduate and postgraduate students to develop a common controlling platform to attain discrete control on source and load side, when multiple sources are acting as input to the converter section. This study aims to provide a decoupled-control analysis in 1- \emptyset , three-wire system which helps the students to understand the concept of DSVM in suppressing the high-frequency current commutation.

Modeling of 1- \emptyset RBI

The simulation diagram of 1- \emptyset RBI is shown in Figure 1 and is modeled using insulated gate bipolar junction transistor (IGBT). The IGBT switches are gated through DSVM technique. The DSVM modulation technique generates a pulse

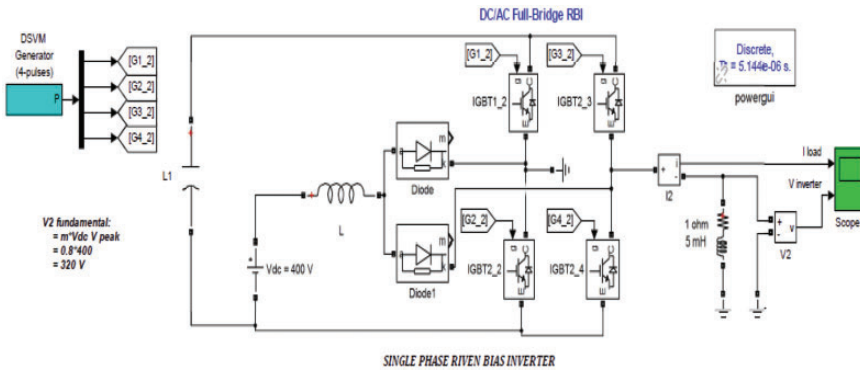


Figure 1. Simulation diagram of I-Ø riven bias inverter. DSVM: digital space vector modulation; IGBT: insulated gate bipolar junction transistor.

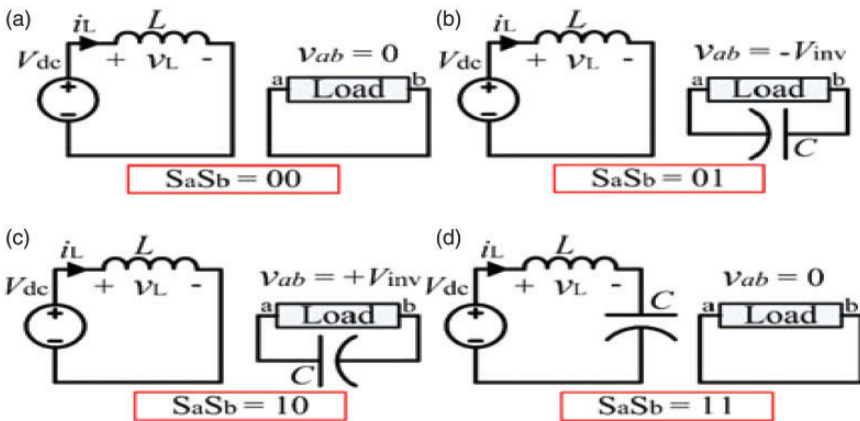


Figure 2. Different switching state configuration of RBI: (a) State 0, (b) State 1, (c) State 2, and (d) State 3.

with a digital code equal to “00,” “01,” “10,” and “11.” The analysis of RBI for different switching technique is shown in Figure 2.

Space averaging analysis of RBI

For the simulated diagram, the following are the state variables

$$U_1 = V_{in}, \quad U_2 = i_{inv} \tag{1}$$

$$x_1 = i_L; \quad x_2 = V_c \tag{2}$$

$$\dot{x}_1 = \frac{di_L}{dt} \quad (3)$$

$$\dot{x}_2 = \frac{dv_c}{dt} \quad (4)$$

During T_{ON}

$$V_{in} = L \frac{di_L}{dt} + i_L R_L \quad (5)$$

$$\frac{di_L}{dt} = \frac{1}{L} V_{in} + \frac{i_L R_L}{L} \quad (6)$$

Voltage across the capacitor

$$V_{inv} = \frac{-1}{C} \int i_{inv} dt \quad (7)$$

$$\frac{dv_{inv}}{dt} = -\frac{1}{C} i_{inv} \quad (8)$$

During T_{off}

$$V_{in} = L \frac{di_L}{dt} + i_L R_L + V_{inv} \quad (9)$$

$$\frac{di_L}{dt} = \frac{1}{L} V_{in} - \frac{i_L R_L}{L} - \frac{V_{inv}}{L} \quad (10)$$

Voltage across the capacitor

$$V_{inv} = \frac{-1}{C} \int i_L dt \quad (11)$$

$$\frac{dv_{inv}}{dt} = -\frac{1}{C} i_L \quad (12)$$

For T_{ON} period, the state space equation is

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} R_L/L & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 1/C \end{bmatrix} u(t) \quad (13)$$

For T_{OFF} period, the state space equation is

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -R_L/L & -1/L \\ 1/C & 0 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 0 \end{bmatrix} u(t) \quad (14)$$

Table 1. RBI state when diode 1 and diode 2.

	Positive half-cycle					Negative half-cycle				
State	0	2	3	2	0	0	1	3	1	0
IGBT 1_2 and IGBT 2_2	0	1	1	1	0	0	0	1	0	0
IGBT 2_3 and IGBT 2_4	0	0	1	0	0	0	1	1	1	0
Diode	FB _{Diode}	RB _{Diode}	FB _{Diode}	RB _{Diode}	FB _{Diode}	FB _{Diode}	FB _{Diode}	FB _{Diode}	FB _{Diode}	FB _{Diode}
Diode 1	FB _{Diode}	FB _{Diode}	FB _{Diode}	FB _{Diode}	FB _{Diode}	FB _{Diode}	RB _{Diode}	FB _{Diode}	RB _{Diode}	FB _{Diode}

IGBT: insulated gate bipolar junction transistor; FB: forward bias; RB: reverse bias.

The average state space model is given in equation (15) and can be linearized by using perturbation algorithm

$$\dot{x}(t) = [(1-d)A_1 + dA_2]x(t) + [(1-d)B_1 + dB_2]u(t) \quad (15)$$

Steady-state analysis

The analysis present in this section is based on the assumptions of ideal component and circuit is operating under steady-state condition. Table 1 provides the information on the state of RBI switches for various biasing conditions of Diodes. The average instantaneous value of voltage in each leg is given in equations (16) and (17)

$$V_a = \begin{cases} (D_{inv} + 1 - D_{conv})V_{inv}, & \text{for } 0 \leq \omega t \leq \pi \\ (1 - D_{conv})V_{inv}, & \text{for } \pi \leq \omega t \leq 2\pi \end{cases} \quad (16)$$

$$V_b = \begin{cases} (-D_{inv} + 1 - D_{conv})V_{inv}, & \text{for } \pi \leq \omega t \leq 2\pi \\ (1 - D_{conv})V_{inv}, & \text{for } 0 \leq \omega t \leq \pi \end{cases} \quad (17)$$

Simulation test results

The SIMULINK illustration of DSVM is exposed in Figure 3. The designed digital modulation gives output pulse with constant duty cycle. The inductor L shown in Figure 1 charges and discharges at constant duty cycle, and hence, current commutation at high frequency is avoided. Table 2 provides the practical considerations and information on grid parameters connected to RB. The DC link voltage is derived as given in equation (18).

$$V_{inv} = \frac{1}{1 - D_{conv}} V_{dc} \tag{18}$$

$$\hat{V}_{ab,1} = mV_{inv} \tag{19}$$

The switches of RBI are operated in under modulation region. The overmodulation operation of the inverter switches is avoided as it introduces high harmonic distortion. Therefore, the duty ratio is bounded to D_{inv} .

It is clear from Figure 4 that current flowing through diode in Figure 2 throbs between 0 and $i_L/2$ while diode 1 in Figure 2 throbs between i_L and $i_L/2$. A comparable investigation of functional to negative half-cycle proves that the diode in Figure 2 beats between i_L and $i_L/2$, while diode 1 in Figure 2 beats between 0 and $i_L/2$. On the other hand, turning on Leg A switches and Leg B switches operating at harmonizing 50 Hz throughout the positive and negative half-phase, the larger incidence current commutation is resolved. As exposed in Figure 4, there is a

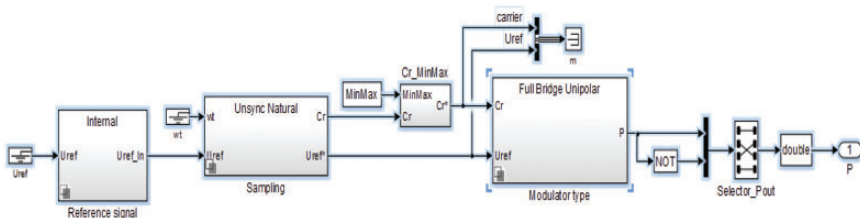


Figure 3. Simulation diagram of DSVM.

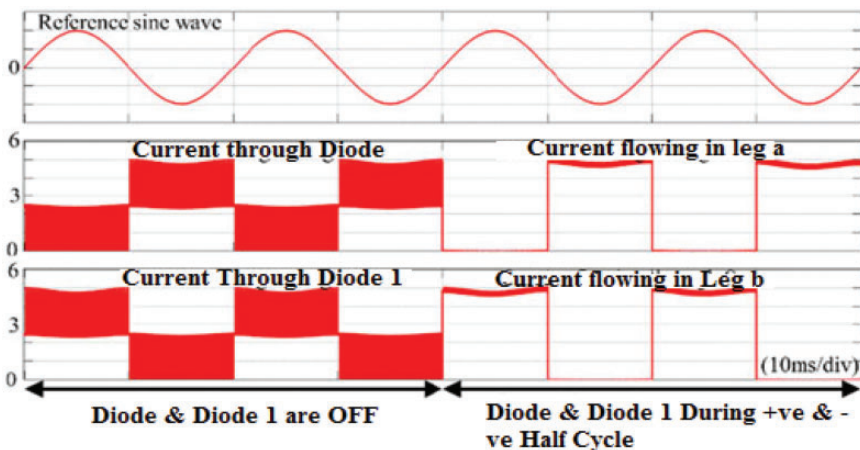


Figure 4. High-frequency commutation eradicated by operating leg A and leg B operating at harmonizing 50 Hz.

wide-ranging drift of inductor current in either of the IGBTs in half-fundamental cycle. Figure 5 shows the complete simulation diagram of riven bias inverter switched with digital space vector modulation. Figure 6 shows the simulation output for the modeling technique of DSVM in comparison with averaging model. The result shown in Figure 7 shows the riven bias inverter output voltage and load current switched by DSVM. Moreover, switching loss is negligible, which in turn indicates that the conduction loss is also negligible.

Parameters of grid connected RBI

The result in Figure 8 shows the total harmonic distortion (THD) analysis of voltage source inverter with Sinusoidal Pulse Width Modulation (SPWM)

Table 2. Grid parameters connected to RBI.

M	0.85 pu
$f_{switching}$	20 KHz
L_f	1.5 mH
$V_{inv(ref)}$	440 V
f_g	60 Hz
r_f	2 Ω
C	220 μ F
L	0.5 mH
R_L	0.1 Ω

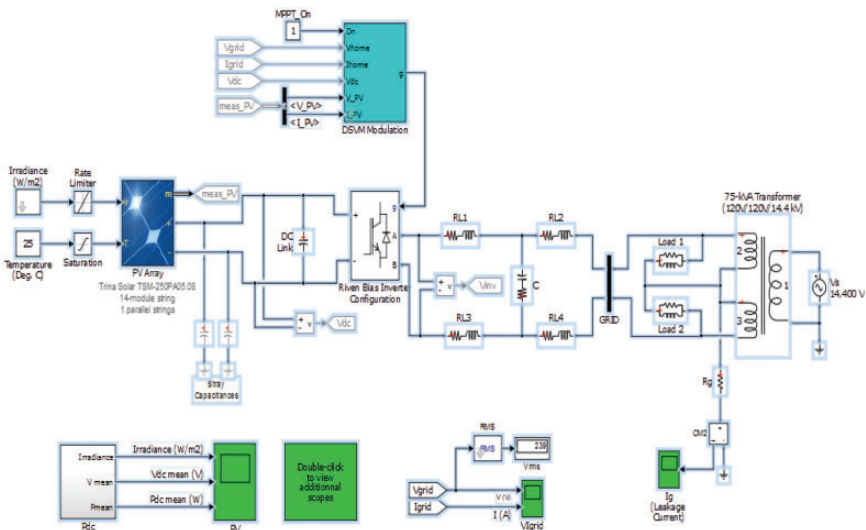


Figure 5. Complete simulation diagram of riven bias inverter. DSVM: digital space vector modulation.

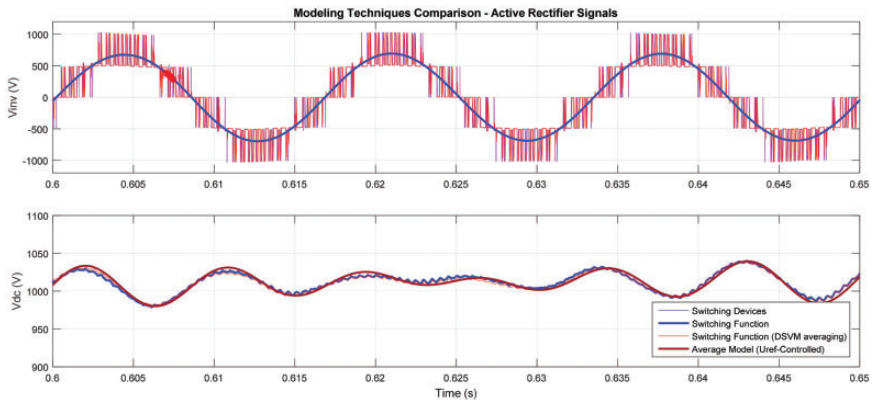


Figure 6. DSVM modeling technique comparison with averaging model.

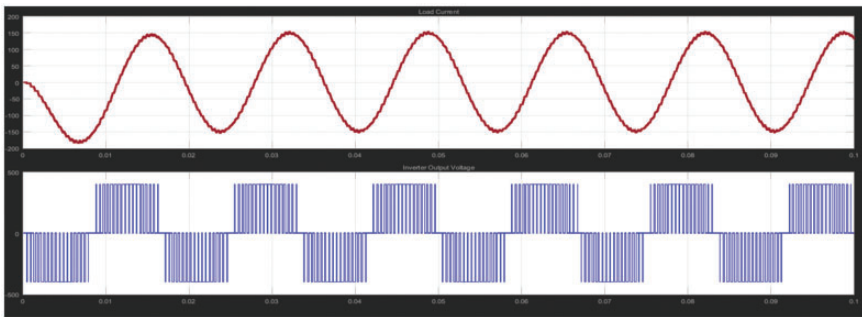


Figure 7. Riven bias inverter output voltage and load current.

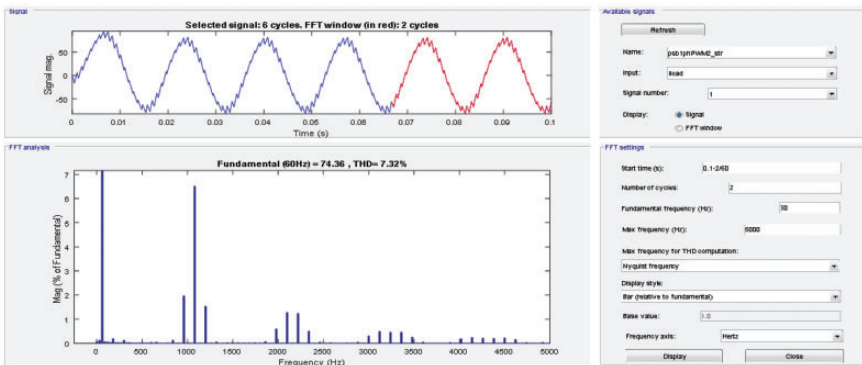


Figure 8. THD analysis of voltage source inverter. THD: total harmonic distortion.

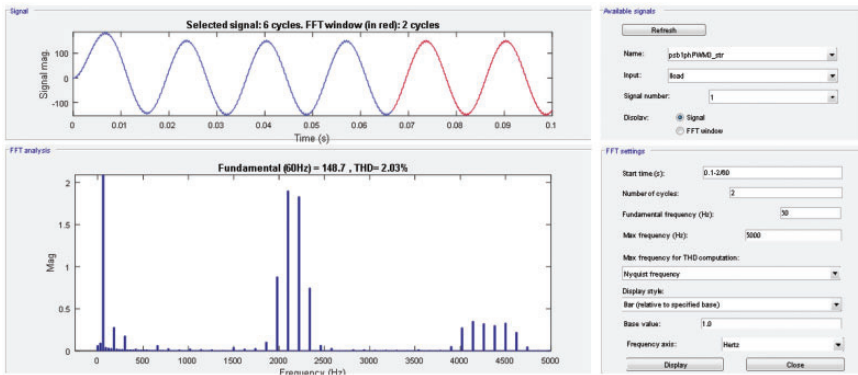


Figure 9. THD analysis of riven bias inverter. FFT: Fast fourier transform analysis.

technique. From Figure 8 at a harmonizing frequency of 60 Hz, the THD is 7.32% for a load current of 100 Amps. Due to this high THD, the high-frequency current commutation is increased which decreases the overall efficiency of the circuit.

The result in Figure 9 shows the THD analysis of RBI with DSVM modulation technique. From Figure 9 at a harmonizing frequency of 60 Hz, the THD is 2.03% for a load current of 150 Amps. From this analysis, it is understood that the high-frequency current commutation is avoided, and hence, the overall efficiency is improved.

Conclusion

The DSVM control technique uses the synchronous reference frame. The single-phase RBI is simulated with MATLAB/SIMULINK with DSVM modulation technique. The designed RBI gives better boost to the inductor charging and discharging with constant duty cycle. The THD analysis is compared between voltage source inverter and RBI and it is observed that the THD is 2.03% in case of RBI, whereas THD is 7.32% for a load current of 150 Amps and 100 Amps, respectively. Hence, it is proved from simulation that the overall efficiency is better and is more than 90% in case of designed RBI with DSVM.

Declaration of Conflicting Interests


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References

1. Abeywardana DBW, Hredzak B and Agelidis VG. An input current feedback method to mitigate the DC-side low-frequency ripple current in a single-phase boost inverter. *IEEE Trans Power Electron* 2016; 31: 4594–4603.
2. Lee SS, Chu B, Idris NRN, et al. Switched battery boost-multilevel inverter with GA optimized SHEPWM for standalone application. *IEEE Trans Ind Electron* 2016; 63: 2133–2142.
3. Diab MS, Elserougi AA, Massoud AM, et al. A pulse-width modulation technique for high voltage gain operation of three-phase z-source inverters. *IEEE J Emerg Sel Topics Power Electron* 2016; 4: 521–533.
4. Siwakoti YP, Peng FZ, Blaabjerg F, et al. Impedance source networks for electric power conversion part I: a topological review. *IEEE Trans Power Electron* 2015; 30: 699–716.
5. Siwakoti YP, Peng FZ, Blaabjerg F, et al. Impedance-source networks for electric power conversion part II: review of control and modulation techniques. *IEEE Trans Power Electron* 2015; 30: 1887–1906.
6. Sahan B, AráUjo SV, Nöding CN, et al. Comparative evaluation of three-phase current source inverters for grid interfacing of distributed and renewable energy systems. *IEEE Trans Power Electron* 2011; 26: 2304–2318.
7. Abdelhakim A, Mattavelli P and Spiazzi G. Three-phase split-source inverter (SSI): analysis and modulation. *IEEE Trans Power Electron* 2016; 31: 7451–7461.
8. Yuvaraja T and Mani G. New Gen Algorithm for Detecting Sag and Swell Voltages in Single Phase Inverter System for Micro grid. *Automatika* 2016; 57: 599–609.
9. Yuvaraja T and Mani G. Fuzzy based analysis of inverter fed micro grid in islanding operation. *Int J Appl Eng Res* 2014; 9: 16909–16916.
10. Yuvaraja T and Mani G. Fuzzy based analysis of inverter fed micro grid in islanding operation – experimental analysis. *IJPEDS* 2015; 5: 464–469.
11. Yuvaraja T and Mani G. Multiple current control strategies for an optimal operation of Vsc linked to an in effectual power system beneath diversified grid condition. *Int J Soft Comput* 2015; 10: 118–126.