



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Report on “Two Days Hands-on Workshop on Semi Custom IC Design Flow from RTL to GDSII using Cadence Tool”

Introduction

The Department of Electronics and Communication Engineering, Sri Sairam College of Engineering, organized a two-day hands-on workshop on “Semi Custom IC Design Flow from RTL to GDSII using Cadence Tool” for final year students and faculty members on 12th and 13th August 2026. The workshop was conducted by Ms. Deepika P, AP/ECE – SSCE, at the IoT Lab from 9.00 AM to 4.00 PM on both days. The objective was to provide practical exposure to the complete Semi Custom IC design flow and enable participants to understand the major stages from RTL design to GDSII generation using Cadence.

Topics and Knowledge Shared

The workshop covered RTL design and functional verification, logic synthesis, floorplanning, placement, clock tree synthesis (CTS), routing, design rule checking (DRC), layout versus schematic (LVS) verification, and GDSII generation. Participants received hands-on exposure to the Cadence design environment and were guided through the sequence of front-end and back-end physical design activities. The sessions emphasized how an RTL design is synthesized, physically implemented, verified, and prepared for GDSII output.

Benefits to Audience

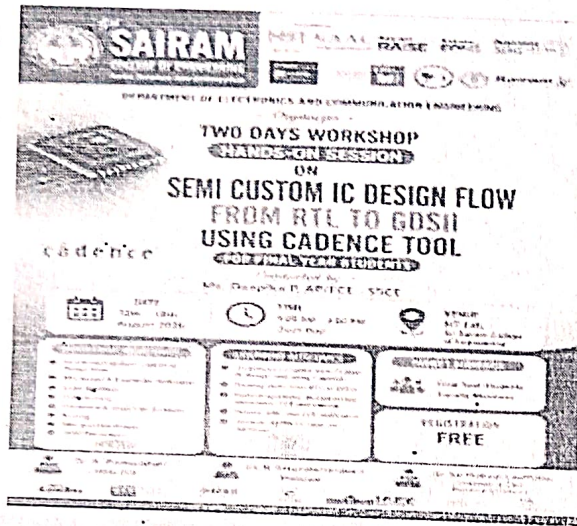
The workshop strengthened participants’ practical understanding of industry-oriented VLSI design practices. Final year students gained useful exposure for their projects, internships, higher studies, and careers in VLSI and semiconductor industries. Faculty members gained familiarity with the Cadence-based flow for laboratory teaching, project guidance, and research activities. The workshop also helped participants connect theoretical VLSI concepts with practical implementation.

Outcome and Conclusion

The two-day workshop successfully enhanced participants’ understanding of the Semi Custom IC design flow from RTL to GDSII. They gained practical knowledge of synthesis, floorplanning, placement, CTS, routing, DRC, LVS, and GDSII generation. Overall, the workshop

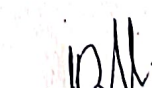
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served as an effective platform for strengthening practical VLSI design skills and encouraging students and faculty members to explore advanced IC design and semiconductor technologies.




 COORDINATOR


 29/08/2026


 28/8/26
 HOD/ECE