

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Report on Hands on Workshop Entitled “Advanced VLSI Physical Design Flow: From Netlist to GDS II”

1. Introduction

The Department of Electronics and Communication Engineering, Sri Sairam College of Engineering, organized a four-day hands-on workshop entitled “Advanced VLSI Physical Design Flow: From Netlist to GDSII” on 15th and 16th August 2026 and 29th and 30th August 2026. The workshop was conducted in association with the IEEE Bangalore Section, IEEE Circuits and Systems Society (CAS), and IEEE Communications Society (ComSoc). The program was designed to provide participants with practical exposure to the complete VLSI physical design flow, beginning with netlist-related concepts and progressing through floor planning, power planning, placement, clock tree synthesis, routing, signal integrity, static timing analysis, physical verification, power analysis, and the transition towards GDS II.

2. Resource Persons

The workshop sessions were handled by the following industry resource persons:

Sl. No.	Resource Person	Designation / Organization
1	Mr. Sohan U	Senior Physical Design Engineer, NVIDIA
2	Mr. Venkata Sai Puneeth Chukka	Backend Implementation Engineer, Microchip Technology

3. Objectives of the Workshop

To introduce participants to the complete VLSI physical design flow from netlist to GDSII.

To provide hands-on understanding of physical design stages and associated design constraints.

To explain practical concepts related to power, performance, area, timing, congestion, and signal integrity.

To familiarize participants with industry-oriented tools, methodologies, and verification practices.

To discuss the role of automation, machine learning, and AI-driven EDA tools in modern physical design.

4. Technical Sessions and Key Learning Focus

The workshop was organized into seventeen technical sessions distributed across four days. The session-wise topics and key learning outcomes are presented below.



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Day	Session	Topic / Activity	Key Learning Focus
Day 1	Session 1	Introduction to ASIC/SoC Flow	Front-end vs. Back-end, Role of a PD Engineer, PPA (Power, Performance, Area)
	Session 2	PNR Flow & Inputs	Logical Libraries (.lib), Physical Libraries (LEF/GDSII), Gate-level Netlist(.v), Constraints (.sdc)
	Session 3	Floorplan & Sanity Checks	Constraint validation, Zero-interconnect delay analysis, Sanity-check scripts
	Session 4	Floor planning	Die/Core area, Aspect Ratio, Utilization, Macro halos, Fly lines, Blockages
Day 2	Session 5	Power Planning	Power Rings, Stripes, Follow-pins, Static vs. Dynamic IR Drop concepts, Electromigration (EM)
	Session 6	Pre-Placement Cells	Well-tap, Endcap, Decap, Tie-high/low, and Filler cell insertion rules
	Session 7	Standard Cell Placement	Global & Detailed Placement, Legalization, Density maps, Congestion mitigation
	Session 8	Post-Placement & MBR	Multi-Bit Register (MBR) banking, post-placement timing/congestion optimization, scan chain reordering
Day 3	Session 9	Clock Tree Synthesis Concepts	Skew, Latency (Insertion Delay), Jitter, Clock Topologies (H-Tree, Mesh)



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	Session 10	CTS Targets Optimization	Clock Buffers/Inverters, Max Transition/Cap, Clock Gating efficiency
	Session 11	Routing (Global Detailed)	Track assignment, Grid routing, DRC Rules, Other Rules, Spacing, Min Area
	Session 12	Signal Integrity (SI) Crosstalk	Glitch, Crosstalk delay, Shielding, NDRs (Non-Default Rules), Buffer insertion
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Day 4	Session 13	Static Timing Analysis (STA)	Setup and Hold checks, Timing paths, Launch/Capture clocks
	Session 14	Physical Verification Tape out	DRC, LVS, ERC, Antenna effect/additional checks, Signoff stream-out
	Session 15	Power Analysis	Static & Dynamic IR drop analysis, Power grid integrity, Vectorless vs. Vector-based power analysis
	Session 16	Industry Guidance Open Discussion	VLSI career roadmap, essential skills (Tel/Python), tools overview, Student Q&A
	Session 17	AI/ML Impact on Physical Design	AI-driven EDA tools (Synopsys DSO.ai, Cadence Cerebrus), machine learning for congestion prediction, PPA optimization, and future career expectations

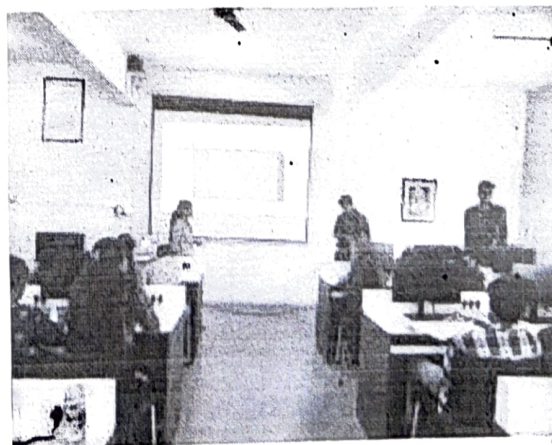
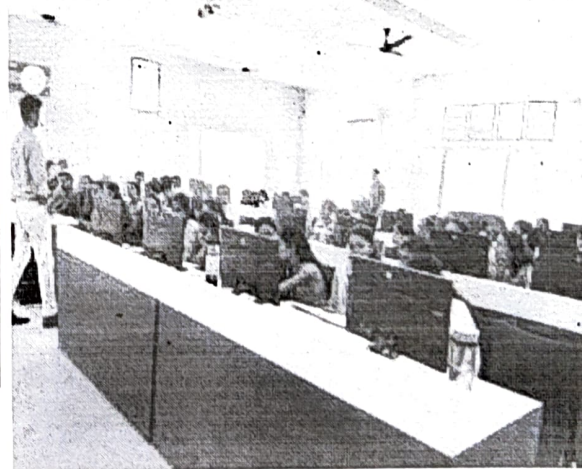
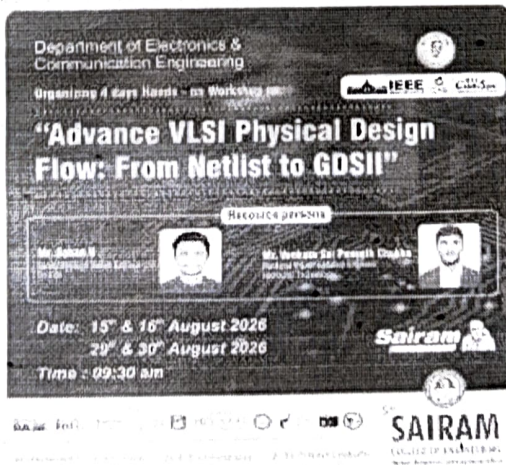
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5. Workshop Activities and Learning Outcomes

The workshop included classroom-based technical explanations and hands-on learning activities in a computer laboratory environment. Participants were introduced to the practical stages of physical design, including floor planning, power planning, placement, clock tree synthesis, routing, timing analysis, and physical verification. The sessions also addressed industry expectations, scripting skills, power and performance optimization, and the emerging role of AI and machine learning in electronic design automation. The program helped participants connect theoretical VLSI concepts with practical backend implementation workflows. The discussions on design constraints, congestion, timing, power integrity, signal integrity, and signoff-related checks provided an integrated view of the physical design process.

6. Photographs of the Workshop

Group Photograph of Participants and Organizers





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7. Conclusion

The four-day hands-on workshop on “Advanced VLSI Physical Design Flow: From Netlist to GDS II” provided participants with structured exposure to the major stages of modern VLSI physical design. The technical sessions and practical discussions strengthened the participants understanding of backend design methodologies, implementation challenges, timing and power considerations, verification requirements, and industry-oriented skills.

Coordinator

Ms. Nithyashree R V

HOD/ECE

Dr. A. Poonguzhali

17/09/2020